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US7154905B2 Case Study Report

This case study reviews how AlphaClaim was used to automatically claim chart 3,000 references in 5 hours to find a high-quality invalidity ground for claim 21 of US7154905B2.

What is AlphaClaim?

AlphaClaim is a "brain" that computes accurate and detailed claim charts for a variety of document types against a given set of claims, adhering to a preponderance of the evidence standard. AlphaClaim has been aligned on 1000s of PTAB IPR institution and final written decisions.

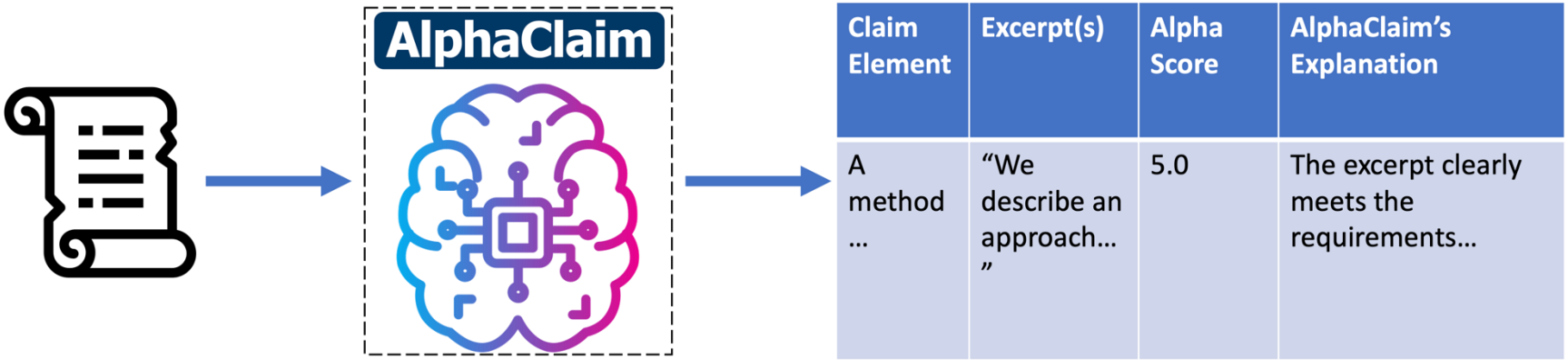
AlphaClaim performs automated, accurate, exhaustive claim charting of **superhuman quantities** of documents (often >10,000). For every document, AlphaClaim produces a claim chart with excerpts and explanations. It then computes an "AlphaScore" out of 5 for each claim element, indicating the strength of the document's disclosure of that element.

AlphaClaim can be applied in three ways. This document focuses on the first.

(1) To **identify the best invalidity grounds** (including combinations), for IPRs.
An AlphaScore of 4 or 5 indicates evidence stronger than the median IPR petition.

(2) To **identify evidence of patent validity** prior to assertion or sale of a patent.
If AlphaClaim's exhaustive review turns up low AlphaScores for all documents, a patent owner can be more confident that the patent will survive IPR or other 102/103 challenges.

(3) To **identify the best evidence of infringement**, for patent owners.
An AlphaScore of 4 or 5 indicates evidence stronger than the median filed claim chart.



Claim Element	Excerpt(s)	Alpha Score	AlphaClaim's Explanation
A method ...	"We describe an approach... "	5.0	The excerpt clearly meets the requirements...

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How does AlphaClaim work?

AlphaClaim leverages many state-of-the-art AI technologies that are used in systems that achieve quality equivalent to the best humans, as detailed in the chart below. While computationally more expensive than consumer-grade chatbots, AlphaClaim achieves high quality with zero hallucination.

	ChatGPT-4	AlphaCode 2	AlphaGeometry	AlphaClaim
Company	OpenAI	Google	Google	AlphaClaim
Purpose	Chatbot	Coding contests	Math Olympiad	Claim charting
Quality Achieved	Mixed	Top 15% of ranked human competitors	Top ~60 mathematicians, worldwide	Skilled IP attorney
Specialization(s)	None	Fine-tuned, sampling-based	Custom pre-train, symbolic engine	Per-element score, sampling, context extraction
Hallucination Rate	Substantial	Zero	Zero	Zero
Computational Complexity	1x	>1,000x	>1,000x	>1,000x

AlphaClaim has 8 patents pending for its technological innovations.

Case & Invalidity Ground Overview

In this report, we show how in a matter of hours, AlphaClaim was able to find a high-quality invalidity ground for claim 21 of the ‘905 patent.

Patent-in-suit (US7154905B2)

Originally issued to Silicon Image with a priority date of 11/22/2000. Currently owned by Universal Connectivity Technologies (UCT). Has been asserted against at least Dell, HP, Lenovo, with all three cases in active litigation. UCT’s argument for infringement of claim 21, according to their claim chart, appears to be that the claim is essential to practicing DisplayPort (either dedicated or over USB), which is widely used to connect laptops to screens (and is a VESA standard). No PTAB cases have been filed against the ‘905 patent yet.

How AlphaClaim was used

We used AlphaClaim to automatically, accurately, exhaustively claim chart approximately 3,000 prior art references. After providing AlphaClaim a claim construction in technical language, which took about 15 minutes, the AlphaClaim process took about 5 hours. AlphaClaim charted all the references we provided it, after it removed grace-period prior art and art already cited during prosecution. By ranking all charted references based on their AlphaScore, AlphaClaim was able to find a high-scoring (5.0/5) single-reference invalidity ground.

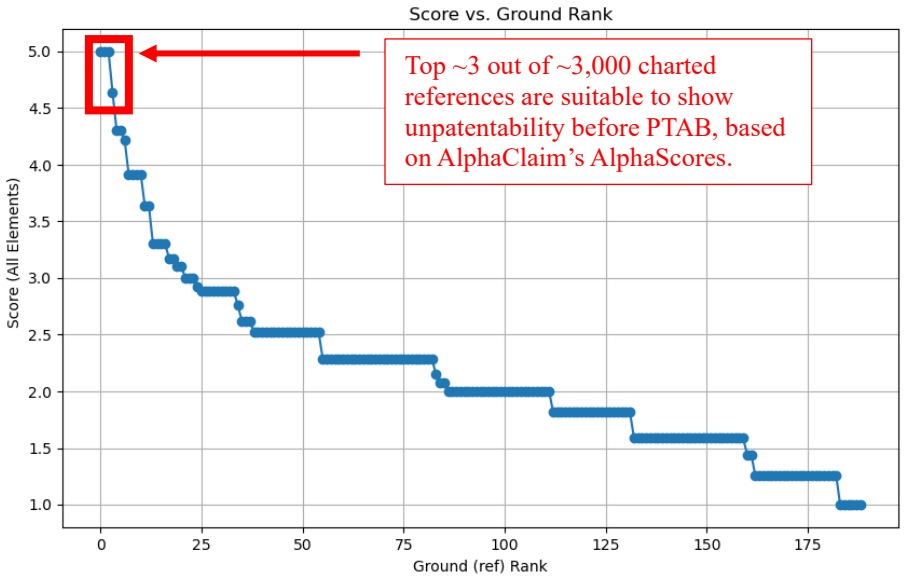
The ground identified

AlphaClaim chose US4542380A (“Method and apparatus for graceful preemption on a digital communications link”), with a priority date of 12/28/1982 and a publication date of 09/17/1985, for its invalidity ground. The reference discloses a method for packet (frame, which AlphaClaim realized is the same thing) preemption on a link controller.

To provide more insight into how AlphaClaim works, we show a score graph for the top 200 references AlphaClaim charted. We then provide the unedited claim chart, AlphaScores, and explanations generated by AlphaClaim for its single-reference ground.

Reviewed Grounds Scores

AlphaClaim works by automatically, accurately, and exhaustively claim charting the prior art provided by the user to find the best invalidity ground possible. The chart shows the results of individual per-reference AlphaScores for the single-reference grounds reviewed in this particular case. While AlphaClaim reviewed ~3,000 references for this case, we terminate the chart at around 200 documents for viewability, as scores drop too low below that. The per-reference AlphaScore is computed as a mean of the per-element AlphaScores within each reference.



AlphaClaim: Generated Claim Chart

This is the unedited output from AlphaClaim. Any legal document (e.g., IPR petition) would be drafted by a professional based on this output.

In this claim chart, AlphaClaim realizes that a "frame" disclosed in the '380 prior art is the same as a "packet" from claim 21. This equivalency is further confirmed by the '905 patent itself, which states in its specification that "when the packet size is small (e.g., 53 bytes in the case of an ATM switch), the spatial relationship of accesses by a single port may not be significant", as ATM uses frames.

Note: the "claim construction" referenced by AlphaClaim is user-provided. This took about 15 minutes to create.

Claim Element (US7154905B2 claim 21)	AlphaClaim's Extracted Excerpt from US4542380A	Alpha-Score	AlphaClaim's Explanation
A communications device for transmitting packets via a communications link, comprising	The function of link controllers 1000 and 2000 is to receive data from the User devices 10, 11, 10' and 11' and to insert that data along with a derived FCS field in the predefined FIG. 2 frame format transmitted on data links 51 and 52. In addition, link controllers 1000 and 2000 receive frames on data links 51 and 52, determine whether the received FCS fields are proper, and extract the data fields for transmission to user devices 10, 11, 10' and 11'. Link controllers 1000 and 2000 also allow a given user device to gracefully preempt the transmission from another user device on links 51 or 52 without requiring the preempted device to retransmit the entire frame.	5.0	1. Communications Device: The Excerpt explicitly mentions link controllers (1000 and 2000) as devices that manage data transmission and reception, fulfilling the requirement of describing a communications device. 2. Transmission of Packets: The Excerpt describes the process of inserting data along with an FCS field into a frame format for transmission, which aligns with the requirement of transmitting packets. 3. Physical Interface or Link: The Excerpt mentions data links (51 and 52) as the medium over which data is transmitted, meeting the requirement of a physical interface or link. It does not specify whether these links are wired or wireless, but the claim construction allows for any kind.
a transmission component that transmits a first packet	processor 1001 determines based on stored information that user device 10 is presently transmitting a frame on link 51, but that user device 11 has priority with respect to user device 10 and that accordingly the user device 10 frame is to be gracefully preempted. Processor 1001 first writes a logic one TAB bit into command register 1220. In response to the TAB bit, transmit control circuit 1301 enters a PREEMPT state 307 ... 05. Upon entering the PREEMPT state 307, circuit 1301 stores the present values of the internal status variables ... N1 in state register 1304 ... 30. T ... he contents of transmit data register 1240, state register 1304, transmit shift register 1305, and FCS shift register 1306 ... es, are conveyed ... 321 to be saved in stack memory 1320. ... 2. Once the contents of transmit data register 1240 have been saved in stack memory 1320, transmit control circuit 1301 ... 05, reinitializes register	5.0	1. The Excerpt explicitly states that a frame being transmitted by user device 10 is preempted for a frame from user device 11 due to the latter having higher priority, meeting the requirement of an ongoing transmission being interrupted for a higher-priority packet. 2. The process is described as graceful, with the preempt state 307 being entered, and the current transmission state being saved in stack memory 1320, aligning with the claim construction of a graceful interruption. 3. The transmission of the higher-priority packet is detailed, with the transmit control circuit 1301 resetting and then transmitting the preempting frame from user device 11. 4. After the transmission of the higher-priority packet, the Excerpt describes the process of resuming the original transmission, with

Claim Element (US7154905B2 claim 21)	AlphaClaim's Extracted Excerpt from US4542380A	Alpha-Score	AlphaClaim's Explanation
	1306 to have an FCS field of 16 logic one bits and then uses the internal status variable ... 52 to effect the transmission by multiplexer 1307 of the PREEMPT character 11111110 ... it. Transmit control circuit 1301 then resets the internal status variables ... N1 and ... returns to the FLAG state 303 and subsequently enters the ADDRESS state 304, the DATA state 305, the FCS state 306 and again the FLAG state 303 as the entire preempting frame from user device 11 is transmitted ... 03. Once the closing flag of the preempting frame ... al, has been transmitted, transmit control circuit 1301 determines ... bit that stack memory 1320 is not empty and based on this determination enters a RESUME state 306. In the RESUME state 306, transmit control circuit 1301 effects the transmission ... 321 of the saved values of the first set of status variables in stack memory 1320 ... on. Then transmit control circuit 1301 controls the transmission of N2 consecutive logic one bits by multiplexer 1307 to replace the logic one bits which were included in the previously transmitted PREEMPT character 11111110.		the transmit control circuit 1301 entering a resume state 306 and restoring the saved transmission state from stack memory 1320.
a preemption component that signals the transmission component to stop transmitting the first packet	When transmit control circuit 1301 determines that a preemption is to occur, it stores the values of the two above-mentioned status variables in a state register 1304. The contents of transmit data register 1240, state register 1304, transmit shift register 1305 and FCS shift register 1306, which contents are referred to collectively herein as a first set of status variables, are then saved in a stack memory 1320 ... 22. When transmit control circuit 1301 determines that the transmission of a preempting frame has been completed, it effects a transmission of the saved values of the set of status variables from stack memory 1320 to the appropriate bit positions of transmit data register 1240, state register 1304, transmit shift register 1305 and FCS shift register 1306 for storage therein and the transmission of the preempted frame can resume from the point of interruption.	5.0	The Excerpt directly addresses the claim construction by detailing a mechanism (transmit control circuit 1301) that effectively interrupts the transmission of a packet (or frame) to allow for the transmission of a preempting frame. This mechanism involves saving the current transmission state (including the contents of the transmit data register 1240, state register 1304, transmit shift register 1305, and FCS shift register 1306) into stack memory 1320. Once the preempting frame's transmission is completed, the saved state is restored, allowing the original transmission to resume from the point of interruption. This process aligns with the claim construction's requirement for a component that informs, signals, controls, or otherwise programs the transmitter to stop transmitting the packet and then resume transmission after an interruption. The Excerpt precisely matches the claim construction by detailing the specific components involved in interrupting and resuming the transmission, including the role of the transmit control circuit 1301 in controlling this process. There is no deviation from the claim construction's requirements, as the Excerpt explicitly states the actions taken to interrupt and then resume the transmission of a packet.

Claim Element (US7154905B2 claim 21)	AlphaClaim's Extracted Excerpt from US4542380A	Alpha-Score	AlphaClaim's Explanation
transmits a preempt indicator indicating that a second packet is to be transmitted	Upon receiving data from user device 11, formatter interface 1011 informs processor 1001 via control bus 1001-CB of its desire to transmit data on data link 51. In response, processor 1001 determines based on stored information that user device 10 is presently transmitting a frame on link 51, but that user device 11 has priority with respect to user device 10 and that accordingly the user device 10 frame is to be gracefully preempted. Processor 1001 first writes a logic one TAB bit into command register 1220. In response to the TAB bit, transmit control circuit 1301 enters a PREEMPT state 307 ... 30. Then the contents of transmit data register 1240, state register 1304, transmit shift register 1305, and FCS shift register 1306, which contents are collectively referred to as the above-mentioned first set of status variables, are conveyed ... 321 to be saved in stack memory 1320. ... 0. Transmit control circuit 1301 ... then uses the internal status variable defining the number, N2, of consecutive ones transmitted on link 52 to effect the transmission by multiplexer 1307 of the PREEMPT character 11111110, also referred to herein. As a start preemption signal.	5.0	The Excerpt precisely matches the claim construction by detailing a scenario where a transmission from user device 10 is preempted in favor of a higher priority transmission from user device 11. It explicitly states that the transmit control circuit 1301 enters a preempt state (preempt state 307) and then transmits a preempt character (11111110), which is used as a start preemption signal. This preempt character serves as the indicator that a different, higher-priority packet is about to be transmitted, fulfilling the claim construction's requirement for an indicator that communicates the initiation of a preemption process for a higher-priority packet. The Excerpt does not infer but explicitly states the process of transmitting a signal to indicate preemption, which aligns with the claim construction. The use of the preempt character as a start preemption signal directly corresponds to the claim construction's requirement for a signal, indicator, symbol, or other message that communicates the preemption of a given packet for a higher-priority transmission.
transmits the second packet	Upon receiving data from user device 11, formatter interface 1011 informs processor 1001 via control bus 1001-CB of its desire to transmit data on data link 51. In response, processor 1001 determines based on stored information that user device 10 is presently transmitting a frame on link 51, but that user device 11 has priority with respect to user device 10 and that accordingly the user device 10 frame is to be gracefully preempted. Processor 1001 first writes a logic one TAB bit into command register 1220. In response to the TAB bit, transmit control circuit 1301 enters a PREEMPT state 307 ... 30. Then the contents of transmit data register 1240, state register 1304, transmit shift register 1305, and FCS shift register 1306, which contents are collectively referred to as the above-mentioned first set of status variables, are conveyed ... 321 to be saved in stack memory 1320. ... 2. Once the contents of transmit data register 1240 have been saved in stack memory 1320, transmit control circuit 1301 writes a logic one TDRE bit into report register 1230. ... 0. Transmit control circuit 1301 clears transmit shift register 1305, reinitializes register 1306 to have an FCS field of 16 logic one bits and then uses the internal status variable defining the number, N2, of consecutive ones transmitted on link 52 to effect the transmission by multiplexer 1307 of the PREEMPT character 11111110, also referred to herein. As a start preemption signal. ... Transmit control circuit 1301 returns to the FLAG state 303 and subsequently enters the ADDRESS state 304, the DATA state 305, the	5.0	The Excerpt precisely matches the claim construction by: 1. Describing the initiation of a preemption process where an ongoing transmission from user device 10 is interrupted in favor of a higher-priority transmission from user device 11. This directly aligns with the claim construction's requirement that a higher-priority packet is transmitted after the original packet's transmission has been interrupted. 2. Mentioning the use of a preempt character (11111110) as a start preemption signal, which aligns with the claim construction for an appropriate interruption or preemption signal/symbol to be sent. The Excerpt explicitly states the process of entering a preempt state (307), saving the current transmission's state in stack memory, transmitting the preempt character as a start preemption signal, and preparing to resume the preempted transmission after the higher-priority packet is sent. This sequence of actions fulfills the claim construction's requirements without deviation or omission.

Claim Element (US7154905B2 claim 21)	AlphaClaim's Extracted Excerpt from US4542380A	Alpha-Score	AlphaClaim's Explanation
	FCS state 306 and again the FLAG state 303 as the entire preempting frame from user device 11 is transmitted in the above-described manner. ... 3. Once the closing flag of the preempting frame, which flag is also referred to herein as an end preemption signal, has been transmitted, transmit control circuit 1301 determines based on the stored stack control circuit 1322 bit that stack memory 1320 is not empty and based on this determination enters a RESUME state 306.		
signals the transmission component to continue transmitting the first packet	Once the closing flag of the preempting frame, which flag is also referred to herein as an end preemption signal, has been transmitted, transmit control circuit 1301 determines based on the stored stack control circuit 1322 bit that stack memory 1320 is not empty and based on this determination enters a RESUME state 306. In the RESUME state 306, transmit control circuit 1301 effects the transmission by multiplexer/demultiplexer 1321 of the saved values of the first set of status variables in stack memory 1320 to the predefined bit positions of transmit data register 1240, state register 1304, transmit shift register 1305 and FCS shift register 1306 via paths 1241, 1311, 1312 and 1313, respectively. Transmit control circuit 1301 reads the contents of state register 1304 via a path 1331 such that its two internal status variables defining the number, N2, of consecutive ones transmitted on link 51 and the number, N1, of bits of a byte that have been shifted by transmit shift register 1305 can be restored to their values at the point of graceful preemption. Then transmit control circuit 1301 controls the transmission of N2 consecutive logic one bits by multiplexer 1307 to replace the logic one bits which were included in the previously transmitted PREEMPT character 11111110. Transmit control circuit 1301 returns to the DATA state 305 and the number of bits in transmit shift register 1305 which were not transmitted prior to preemption are now shifted out via multiplexer 1307 onto data link 51. Formatter interface 1010 can now resume transferring bytes to transmit data register 1240 and the balance of the preempted frame from user device 10 can be transmitted on data link 51 in the above-described manner.	5.0	The Excerpt precisely matches the claim construction in several key aspects: 1. It states that after the end preemption signal of a preempting frame is transmitted, the transmit control circuit 1301 detects that the stack memory 1320 is not empty and enters the RESUME state 306, which aligns with the requirement for a mechanism to control the transmitter to resume the original packet's transmission. 2. The process of resuming the transmission involves the restoration of saved status variables and the continuation of the preempted frame's transmission from where it was interrupted, without retransmitting the bytes that went through before the interruption. This directly fulfills the claim construction's requirement that the resumption explicitly indicates that the original packet's transmission continues from the point of interruption without retransmission of previously transmitted bytes. 3. The Excerpt explicitly mentions the transmission of the saved values of the first set of status variables and the continuation of the preempted frame's transmission, which is a clear indication of a resumption as defined by the claim construction. The Excerpt does not deviate from the claim construction in any significant way. It provides a detailed description of the process that matches all the requirements outlined by the claim construction.
wherein packets include in-band symbols and the indicators include one or more out-of-band symbols	Link controller 1000 then saves the values of a first set of status variables which collectively define the present status of link controller 1000 and transmits a PREEMPT character 11111110 (FIG. 3) followed by a complete frame including the data from user device 11. After the closing flag of the preempting frame has been transmitted, the saved values of the first set of status variables are used to return link	5.0	The Excerpt explicitly mentions the transmission of a PREEMPT character (11111110), which aligns with the claim construction's requirement for an out-of-band signal that cannot normally occur in regular packet data. This character is used to indicate the initiation of a preemption process, which is a clear indication of a unique encoding scheme for interruption or preemption signals.

Claim Element (US7154905B2 claim 21)	AlphaClaim's Extracted Excerpt from US4542380A	Alpha-Score	AlphaClaim's Explanation
	controller 1000 to its status at the point the preempted frame was interrupted ... me. Upon detecting the PREEMPT character, link controller 2000 saves the values of a second set of status variables which collectively define the present status of link controller 2000. ... e. Since multiplexer 1307 transmits the PREEMPT, ABORT and FLAG characters under the control of transmit control circuit 1301 rather than by conveying bits transmitted by transmit shift register 1305 or FCS shift register 1306, no dummy logic zero bits are inserted in		Additionally, the Excerpt describes the role of the multiplexer 1307 and transmit control circuit 1301 in controlling the transmission of the PREEMPT character without the insertion of dummy logic zero bits, further emphasizing the unique handling of this signal compared to regular data transmission. This handling ensures the PREEMPT character's distinctiveness from regular packet data, fulfilling the claim construction's criteria.